APPENDIX

Changes to Claims:

The following are marked-up versions of the amended claims:

Fig 9

1. (Twice Amended) A piezoelectric device, comprising:

a semiconductor integrated circuit having a plurality of bumps formed thereon; and

a piezoelectric resonator element, the semiconductor integrated circuit and the piezoelectric resonator element being included in a package,

the semiconductor integrated circuit being mounted in a center of an opening formed in a center of a base, and the semiconductor integrated circuit being connected to an input/output electrode pattern on the base through the plurality of bumps, and wherein the base includes a layered part, which surrounds the semiconductor integrated circuit, for mounting the piezoelectric resonator element, the layered part comprising at least two layers, including a first layer and a second layer, the first layer being below the second layer, wherein an opening of the first layer is formed to be larger than an opening of the second layer.

Fig 11 #31 ?

14. (Twice Amended) A piezoelectric device, comprising:

a semiconductor integrated circuit; and

a piezoelectric resonator element, the semiconductor integrated circuit and the piezoelectric resonator element being included in a package,

a plurality of bumps being formed at two opposing sides of an active element surface of the semiconductor integrated circuit, the semiconductor integrated circuit being mounted in an opening formed in a center of a base, and the semiconductor integrated circuit being connected to an input/output electrode pattern of the base through the plurality of

bumps, and a protrusion being formed in at least one side wall of the base facing the side of the semiconductor integrated circuit and protruding into the opening to form the protrusion.

22. (Twice Amended) A piezoelectric device, comprising:

a semiconductor integrated circuit; and

a piezoelectric resonator element, the semiconductor integrated circuit and the piezoelectric resonator element being included in a package,

a plurality of bumps being formed at two opposing sides of an active element surface of the semiconductor integrated circuit, the semiconductor integrated circuit being mounted in a center of an opening formed in a center of a base, and the semiconductor integrated circuit being connected to an input/output electrode pattern through the plurality of bumps by ultrasonic bonding, each of the plurality of bumps formed on the semiconductor integrated circuit being shaped to have two levels, a first level having a diameter 0.8 to 0.9 times and a second level having a diameter 0.4 to 0.45 times the length of an opening in a pad provided on the active element surface of the semiconductor integrated circuit.

26. (Twice Amended) The piezoelectric device according to claim 2225, ~~each of the plurality of bumps formed on the semiconductor integrated circuit being shaped to have two levels, a~~ wherein the first level is~~being~~ 80 to 90 μm in diameter and 30 to 35 μm in height, and the~~a~~ second level is~~being~~ 40 to 45 μm in diameter and 30 to 35 μm in height.